**Aditya Institute of Technology and Management (Autonomous), Tekkali**

**Subject: Algorithms for VLSI Design Automation Subject Code: 16MVL1010**

**Name of the faculty: Harihara Santosh Dadi Year: I Semester: II**

**Branch: M.Tech. (VLSI) Academic Year: 2017 – 2018**

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| **Periods** | **Date**  **(Tentative)** | **Topic** | **Unit No** | **Teaching Methodology** | **Remarks** | **Corrective Action Upon Review** |
| 1 | 26/2/18 | PRELIMINARIES: | I | BB |  |  |
| 2 | 27/2/18 | Introduction to Design Methodologies, | BB |  |  |
| 3 | 28/2/18 | Design Automation tools | BB |  |  |
| 4 | 5/3/18 | BB |  |  |
| 5 | 6/3/18 | Algorithmic Graph Theory | BB |  |  |
| 6 | 7/3/18 | BB |  |  |
| 7 | 8/3/18 | Computational Complexity | BB |  |  |
| 8 | 12/3/18 | BB |  |  |
| 9 | 13/3/18 | Tractable and Intractable Problems | BB |  |  |
| 10 | 14/3/18 | BB |  |  |
| 11 | 15/3/18 | GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION | II | BB |  |  |
| 12 | 19/3/18 | Backtracking | BB |  |  |
| 13 | 20/3/18 | Branch and Bound | BB |  |  |
| 14 | 21/3/18 | Dynamic Programming | BB |  |  |
| 15 | 22/3/18 | Integer Linear Programming | BB |  |  |
| 16 | 26/3/18 | Local Search | BB |  |  |
| 17 | 27/3/18 | Simulated Annealing | BB |  |  |
| 18 | 28/3/18 | Tabu search | BB |  |  |
| 19 | 2/4/18 | BB |  |  |
| 20 | 3/4/18 | Genetic Algorithms | BB |  |  |
| 21 | 4/4/18 | Layout Compaction | III | BB |  |  |
| 22 | 5/4/18 | BB |  |  |
| 23 | 9/4/18 | Placement | BB |  |  |
| 24 | 10/4/18 | Floor planning | BB |  |  |
| 25 | 11/4/18 | Routing Problems | BB |  |  |
| 26 | 12/4/18 | Concepts and Algorithms MODELING AND SIMULATION | BB |  |  |
| 27 | 16/4/18 | Gate Level Modeling and Simulation | BB |  |  |
| 28 | 17/4/18 | BB |  |  |
| 29 | 18/4/18 | Switch level Modeling and simulation | BB |  |  |
| 30 | 19/4/18 | BB |  |  |
| 31 | 23/4/18 | LOGIC SYNTHESIS AND VERIFICATION | IV | BB |  |  |
| 32 | 24/4/18 | Basic issues and Terminology | BB |  |  |
| 33 | 25/4/18 | Binary –Decision diagram | BB |  |  |
| 34 | 26/4/18 | Two – Level Logic Synthesis | BB |  |  |
| 35 | 1/5/18 | HIGH LEVEL SYNTHESIS | BB |  |  |
| 36 | 2/5/18 | Hardware Models | BB |  |  |
| 37 | 3/5/18 | Internal representation of the input algorithm | BB |  |  |
| 38 | 11/6/18 | Allocation | BB |  |  |
| 39 | 12/6/18 | Assignment and Scheduling | BB |  |  |
| 40 | 13/6/18 | Some Scheduling Algorithms | BB |  |  |
| 41 | 14/6/18 | Some aspects of Assignment problem | BB |  |  |
| 42 | 18/6/18 | High – level Transformations | BB |  |  |
| 43 | 19/6/18 | PHYSICAL DESIGN AUTOMATION OF FPGA’S | V | BB |  |  |
| 44 | 20/6/18 | FPGA technologies | BB |  |  |
| 45 | 21/6/18 | Physical Design cycle for FPGA’s partitioning and routing for segmented and staggered models | BB |  |  |
| 46 | 25/6/18 | BB |  |  |
| 47 | 26/6/18 | BB |  |  |
| 48 | 27/6/18 | BB |  |  |
| 49 | 28/6/18 | BB |  |  |
| 50 | 2/7/18 | BB |  |  |
| 51 | 3/7/18 | BB |  |  |
| 52 | 4/7/18 | BB |  |  |
| 53 | 5/7/18 | PHYSICAL DESIGN AUTOMATION OF MCM’S: | VI | BB |  |  |
| 52 | 9/7/18 | MCM technologies | BB |  |  |
| 53 | 10/7/18 | MCM physical design cycle | BB |  |  |
| 54 | 11/7/18 | Partitioning, Placement | BB |  |  |
| 55 | 12/7/18 | Chip array based and full custom approaches | BB |  |  |
| 56 | 16/7/18 | Routing – Maze routing | BB |  |  |
| 57 | 17/7/18 | Multiple stage routing | BB |  |  |
| 58 | 18/7/18 | Topologic routing, Integrated Pin – Distribution and routing | BB |  |  |
| 59 | 19/7/18 | routing and programmable MCM’s | BB |  |  |

Signature of the faculty Signature of HOD/ECE